Navy Case No. 74023

PROGRAMMABLE GRAY-SCALE LIQUID CRYSTAL DISPLAY

Cross Reference to Related Applications

This application is a continuation-in-part ~~continuation~~ under 37 CFR 1.53 of co-pending U. S. Patent Application Serial no. 08/301,170, "Electrically Addressable Silicon-On-Sapphire Light Valve", R. L. Shimabukuro et al.

Background of the Invention

The present invention relates to liquid crystal displays formed on silicon-on-sapphire. More specifically, but without limitation thereto, the present invention relates to a liquid crystal display integrated with electronic circuitry on the display to provide a programmable gray-scale and to compensate for nonuniform and non-operating pixels in the display.

Liquid crystal displays (LCDs) are used in a wide variety of commercial applications, including portable and laptop computers, wristwatches, camcorders, and television screens.

Inherent limitations of existing technology arise from the necessity of fabricating LCDs on transparent glass or quartz substrates which are not amenable to processing with high quality electronic materials.

The integration of drive circuitry with LCDs has improved reliability and reduced size and weight for portable applications, but has been limited to thin film transistor technology using, for example, amorphous (α-Si) and polycrystalline (poly-Si) silicon deposited on glass and quartz substrates.

Lattice and thermal mismatch between layers and low temperature deposition methods used in thin film transistor technology result in a silicon layer with poor charge carrier mobility and crystallographic defects which are directly related to electronic device performance and limitations. A comparison of MOS technologies for active matrix LCDs is shown in the following table:

	POLY-TFT HT-CMOS	POLY-TFT MT-CMOS	α-Si:H NMOS	CMOS UTSOS
1. Substrate	fused quartz	hard glass	hard glass	Al_2O_3
2. Max. process temp	~1000°C	600°C	300°C	1000°C
3. Threshold (Volts)(n-chnl)	2.0	2.0	1.5	0.5
4. Mobility	100	40	0.75	380
5. Shift register	20 MHz @15V	5 MHz @15V	0.1MHz @15V	>100MHz @5V
6. Integrated LSI logic	N/A	N/A	N/A	yes

For ultra-high resolution display applications, the high density of LSI circuitry is of particular importance for integrated displays. Compatibility with Very Large Scale Integration (VLSI) allows integration on-chip of video drivers, digital logic, compensating or fault-tolerant circuitry, and other computational circuitry, thereby providing greater functionality, higher reliability, and improved performance. A need thus exists for a material quality that overcomes the problems which occur in small scale, high density circuitry fabricated in α-Si and poly-Si.

A need also exists for multiple level gray-scale and color displays for the applications mentioned above. Color displays have been made with colored filters by incorporating dyes into a guest host matrix, or by using field sequential color techniques. Color liquid crystal displays may also be made using the gray-scale properties of a liquid crystal display to achieve variations in color.

While the optical, electrical, and electro-optical properties of the liquid crystal material primarily determine the gray-scale properties, the substrate plays a significant role in the pixel uniformity of the display. Substrate warpage, or variations in surface morphology, can lead to variations in thickness of the liquid crystal layer. This in turn may lead to a nonuniform display intensity for a given pixel voltage, which is a problem for multiple gray-scale displays, high density

displays, and displays having stringent operating requirements. Furthermore, for high brightness displays, substantial heating may occur which can not be readily dissipated through substrates such as glass or quartz.

Prior research on brightness nonuniformity of LCDs established another cause of display nonuniformity, specifically the high resistance of narrow electrodes in high density LCDs.

A related problem particularly important for displays having stringent specifications is fault tolerance, or recovering from failed pixels. This problem is not emphasized in an LCD market primarily interested in low cost commercial applications, but becomes significant in high-reliability technology.

Another problem is that as display resolutions increase, the number of switching elements required in active matrix displays increases. A higher number of switching elements causes yield problems in manufacturing and in reliability. Fabrication yields of nonlinear switching elements (thin film transistors or diodes) may be improved by redundancy, but the redundancy applies only to the switching element rather than for the entire pixel.

Summary of the Invention

The programmable gray-scale LCD of the present invention is directed to overcoming the problems described above, and may provide further related advantages. The following description of a programmable gray-scale LCD does not preclude other embodiments and advantages of the present invention that may exist or become obvious to those skilled in the art.

A programmable gray-scale liquid crystal display comprises a polarizer operably coupled to a beam of incident light to pass a beam of polarized light having a polarization axis. A sequence of liquid crystal display pixels serially aligned with the beam of polarized light controls the angle of the polarization axis. An analyzer passes a gray-scale portion of the beam of polarized light from the sequence of liquid crystal display pixels corresponding to the angle of the polarization axis. Each pixel in the sequence may be independently programmed to vary the angle of the polarization axis for calibrating the display to a standard gray-scale and for correcting faulty pixels with VLSI on-chip driver and interface circuits.

One advantage of the programmable gray-scale LCD is that it provides a gray-scale with high resolution.

Another advantage is that multiple level gray-scale and color displays may be made according to the present invention.

Still another advantage is that failed pixels may be corrected by reprogramming the display.

Yet another advantage is that the gray-scale of the display may be programmed to conform to a gray-scale standard.

Another advantage is that a plurality of liquid crystal pixels are concatenated to form a display having a gray-scale that is programmable and fault-tolerant.

The features and advantages summarized above in addition to other aspects of the present invention will become more apparent from the description, presented in conjunction with the following drawings.

Brief Description of the Drawings

Fig. 1 is a diagram of an example in the prior art of a liquid crystal display pixel in the non-transmissive or OFF state.

Fig. 2 is a diagram of the liquid crystal display pixel of Fig. 1 in the transmissive or ON state.

Fig. 3 is a diagram of the liquid crystal display pixel of Fig. 1 with gray-scale control.

Fig. 4 is an exploded view diagram of a programmable gray-scale LCD of the present invention.

Fig. 5 is a flow chart of the method of the present invention for fabricating the LCD of Fig. 4.

Fig. 6 is a block diagram of an optical testbed used for programming the LCD of Fig. 4.

Fig. 7 is a flow chart of gray-scale calibration programming of the LCD of Fig. 4 in the test bed of Fig. 6.

Fig. 8 is a flow chart of fault tolerance programming of the LCD of Fig. 4 in the test bed of Fig. 6.

Description of the Invention

The following description is presented solely for the purpose of disclosing how the present invention may be made and used. The scope of the invention is defined by the claims.

Figs. 1-3 are diagrams illustrating an example of liquid crystal display (LCD) gray-scale as currently practiced. In Fig. 1, a liquid crystal medium 10 is contained within transparent electrodes 12 to form a pixel element 14. Pixel element 14 is then placed between a polarizer 16 and an analyzer 17. Analyzer 17 polarizes light in a direction orthogonally oriented with polarizer 16. When unpolarized light from a light source 22 passes through polarizer 16, transparent electrodes 12, and liquid crystal medium 10, the light becomes polarized and is absorbed by analyzer 17. Pixel element 14 consequently appears OFF or opaque.

In Fig. 2, closing a switch 20 causes the application of a voltage V from a voltage source 18 to transparent electrodes

12. Voltage V causes the orientation of liquid crystal medium 10 to change, which rotates the polarization axis of the light from light source 22 passing through polarizer 16. The rotated polarization axis allows the light to pass through analyzer 17. Pixel element 14 consequently appears ON or transparent.

In Fig. 3, voltage V is varied to vary the rotation of the polarization axis of the light from light source 22. The percentage of light from light source 22 passing through analyzer 17 may thus be controlled, resulting in a gray-scale varying from transparent to opaque. Typical LCDs are fabricated from a plurality of pixel elements 14, usually in a two-dimensional array or display area. A variation of this concept includes the design of pixel elements in a liquid crystal medium that are in the OFF state or opaque when there is no voltage applied to the transparent electrodes. Another variation uses bistable ferroelectric liquid crystals (FLCs), which have a continuously variable polarization with application of a voltage. FLC's may exhibit a gray scale by rapidly switching the pixels to allow a time averaged optical state which corresponds to a gray level. When used for color generation, the FLC pixel switching is correlated with the desired wavelength of light. This method is referred to as field sequential color.

The embodiment described herein pertains to nematic liquid crystals, however FLC's, supertwisted nematic, and the like may

also be used to practice the present invention.

Fig. 4 is a diagram of a fault tolerant, programmable gray-scale LCD 40 of the present invention with silicon-on-sapphire (SOS) technology to provide the advantage of VLSI compatibility. In this exploded view, spacers 44 form a cavity between SOS wafers 42. Pixel element electrodes are formed in SOS wafers 42A, 42B, and 42C. SOS wafers 42A, 42B, and 42C are referred to collectively as SOS wafers 42. The cavity formed by SOS wafers 42 and spacers 44 are filled with an appropriate liquid crystal material 10, such as nematic, supertwisted nematic or ferroelectric liquid crystals, and interposed between SOS wafers 42. Exemplary techniques for fabricating SOS wafers 42 are described by S. S. Lau et al in U.S. Patent 4,177,084, "Method For Producing a Low Defect Layer of Silicon-on-Sapphire Wafer", incorporated herein by reference thereto. SOS wafers 42 provide drive control and pixel electrodes for liquid crystal material 10. Each of SOS wafers 42 may be fabricated independently and joined in the final steps of fabrication. The combination of spacers 44 and SOS wafers 42 results in a serial arrangement of pixels in optically coupled independent displays. The pixels may be individually programmed to calibrate a uniform gray-scale and to provide redundancy for replacing faulty pixels.

Fig. 5 is a flow chart of the process for fabricating LCD 40. Portion "A" lists the order of steps in the fabrication of

SOS wafers 42 comprising the integrated drive control and pixel electrode circuitry. The drive control electronics may include circuitry to detect failure conditions in the display, to calibrate the display gray-scale, or to switch to alternative pixel configurations for replacing defective pixels. The circuitry need not be identical on each of SOS wafers 42, but preferably includes common drive and interface circuitry. Portion "B" of Fig. 5 describes the fabrication of the pixel electrodes on SOS wafers 42A and 42C and insertion of spacers 44.

Portion "C" of Fig. 5 lists the order of steps for fabricating the pixel electrodes on SOS wafer 42B.

Portion "D" of Fig. 5 lists the order of steps for joining SOS wafers 42 and spacers 44 to form LCD 40.

Referring now to Figs. 4 and 5, SOS wafers 42A and 42C in Fig 4 are formed of device quality silicon-on-sapphire. Well known techniques are used to form VLSI circuitry (not shown) in the steps of isolation photo and etch, channel implant, gate oxidation, poly deposition and doping, gate definition, source/drain implant and annealing, oxide deposition and contact etch, metal deposition, patterning, and sintering, and deposition and patterning of passivation oxide. The VLSI circuitry may be formed on SOS wafers 42 outside of a display region 11.

A transparent conductor, such as indium tin oxide, tin

oxide, or polysilicon is deposited on substrates 42A and 42C in display region 11 and pixel electrodes (not shown) are patterned according to well known techniques. Spacers 44, schematically shown in Fig. 4, are then attached to substrates 42B and 42C. Spacers 44 may be, for example, glass beads randomly distributed on the substrate.

A transparent conductor is deposited on opposite sides of a polished blank sapphire wafer or alternately glass, quartz or other transparent material to form SOS wafer 42B. The transparent conductor may then be patterned and formed into pixel electrodes (not shown).

Spacers 44 are inserted to form cavities on SOS wafers 42. The cavities are then filled with liquid crystal material 10. The pixel elements on each of display regions 11 of SOS wafers 44 are serially aligned to form pixel sequences, and SOS wafers 42 and spacers 44 are assembled into a single structure. The assembly of LCD 40 is completed with the addition of polarizer 16 and analyzer 17 of Fig. 1 using techniques well known to those skilled in the art.

LCD 40 may be programmed and calibrated in an optical test bed 70 as shown in the block diagram of Fig. 6. A light source 702 transmits a beam of light having a spatially uniform intensity pattern through intensity homogenizing and projection optics 704 to LCD 40. The light passed by LCD 40 is focused by imaging optics 706 and measured by an optical detector 708.

Programming electronics 710 adjusts programming voltages V_1 and V_2 to vary the gray-scale to a desired value as measured by optical detector 708 for each pixel sequence of LCD 40.

Fig. 7 is a flow chart of a program for calibrating LCD 40 to a standard gray-scale. LCD 40 is placed into optical test bed 70 of Fig. 6 and subjected to light from light source 702. Voltage V_1 is applied to a pixel of one of the independent displays of LCD 40 corresponding to a gray-scale or color value. The percentage of light passed through the selected pixel is measured by optical detector 708 and compared to a standard. If the measured value is within tolerance of the standard value, voltage V_2 is fixed to maintain the calibrated pixel intensity and voltage V_1 is applied to another pixel sequence. If the measured value lies outside the tolerance of the standard value, V_2 and/or V_1 may be adjusted to vary the percentage of light passed to optical detector 708 until the measured value is within tolerance. Each row and column of LCD 40 may be calibrated in a similar manner. After LCD 40 has been calibrated for one gray-scale level or color, another level or color is selected and the calibration is repeated until all rows and columns of LCD 40 are calibrated for all gray-scale levels or colors of the standard.

Fig. 8 is a flow chart of a program for correcting faulty pixels. LCD 40 is placed into optical test bed 70 of Fig. 6 and subjected to light from light source 702. While Voltage V_1 is

applied to a pixel in a pixel sequence of LCD 40, the light passing through the pixel is measured and compared with a standard value. If the measurement falls outside the specification tolerance, voltage V_2 is applied to another pixel in the pixel sequence. Voltage V_2 is then adjusted in increments until the measured light passing through the pixels falls within the specified tolerance. Once the desired value is achieved, V_2 is fixed for the corresponding pixel. Each pixel in the display area may be similarly calibrated.

Monolithically integrated, i.e. on-chip, VLSI circuitry may be fabricated according to well-known techniques outside region 11 of SOS wafers 42 in Fig. 4. The VLSI circuitry may include memory circuits such as static random access memory (SRAM), dynamic RAM (DRAM), and non-volatile RAM (NVRAM) to store the calibration information obtain through the processes described in Fig. 7 and Fig. 8.

Other modifications, variations, and applications of the present invention may be made in accordance with the above teachings other than as specifically described to practice the invention within the scope of the following claims.